

# Virtuoso Analog Design Environment



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<b>Title:</b>	Virtuoso Analog Design Environment - v5.1.41	<b>Type:</b>	Instructor Led Course
<b>Product Number:</b>	82083	<b>Price:</b>	\$ 2,800.00 <a href="#">Refund Policy</a>
<b>Length:</b>	4 Day(s)		
<b>Category:</b>	Evaluating Simulation Results Extracted Parasitic Analysis Mixed-Signal Simulation DC, AC, and Transient Simulation Hierarchical Design Back End Front End System Modeling and Design Methodology Chip Design Analog Design		
<b>Description:</b>	<p>By taking this course, you'll learn front-to-back design flow with the Virtuoso® Analog Design Environment system. You will start with a top-level block description of your design, build schematics, run simulations, and utilize the entire Virtuoso Analog Design Environment.</p> <p>By using a series of simulation tools, you will verify circuit operation over process corners, optimize component values, and accurately predict production yield. Afterwards, you will learn to use the environment to write and then execute automated simulation runs, finishing the design flow with layout parasitic extraction and simulation.</p>		
<b>Learning Objectives:</b>	<p>Upon completion of this course, the student will be able to:</p> <ul style="list-style-type: none"><li>• Use the Cadence® Design Framework II environment</li><li>• Simulate circuits with the Virtuoso® Spectre Circuit Simulator</li><li>• Run analog behavioral (AHDL) simulations with the Verilog®-A simulator</li><li>• Capture a schematic of a BiCMOS amplifier with the Virtuoso® Schematic Editor</li><li>• Use the Schematic Editor Symbol Generator to create symbols for your schematics</li><li>• Netlist and simulate a BiCMOS amplifier</li><li>• Analyze simulation results with the Waveform Window and the WaveScan tool</li><li>• Run parametric analysis</li><li>• Simulate over process corners using the Corners Analysis tool</li><li>• Perform sensitivity analysis</li><li>• Run batch simulations with Open Command Environment for Analysis (OCEAN)</li><li>• Create new components using the Component Description Format (CDF)</li><li>• Simulate with ideal macromodels</li><li>• Use <i>inline</i> subcircuits to simulate components with parasitic models</li><li>• Use inherited connections to reprogram a wired connection by instantiated property</li><li>• Use the Hierarchy Editor to configure a design hierarchy with different cell views</li><li>• Run Monte Carlo and optimization analyses</li><li>• Perform layout parasitic extraction and simulate the circuit with parasitics</li></ul>		
<b>Software:</b>	Virtuoso® Layout Editor LVS LPE Verilog-A simulator Virtuoso® Spectre Circuit Simulator Virtuoso® Analog Circuit Optimizer Option Virtuoso® Analog Corners Analysis Option Virtuoso® Analog Design Environment Cadence® Design Framework II OCEAN Virtuoso® Schematic Editor		
<b>Agenda:</b>	<b>Day 1</b>		

Introduction and design flow overview

- Top-down simulation, including analog behavioral modeling
- Capturing the schematic of a BiCMOS operational amplifier
- Setting up the analog simulation environment
- Running simulations with the Virtuoso® Spectre Direct simulator
- Analyzing simulation results
- Exploring the Waveform Window features
- Using the WaveScan Tool
- Saving and restoring simulation states
- Annotating simulation results in the schematic

## Day 2

Using the Waveform Calculator to measure the simulation results

- Backing up simulation data
- Using the Results Browser
- Using the Print Engine/Conditional Search tool
- Exploring Virtuoso® Spectre sweep features
- Using OCEAN and SKILL
- Running Virtuoso® Spectre MDL
- Analyzing dcmatch, and transient operating point results
- Using the Component Description Format (CDF)

## Day 3

Running simulations with subcircuits and macromodels

- Using inline subcircuits
- Set up and run Parametric Analysis
- Using the Corners Analysis tool
- Running Monte Carlo Analysis
- Exploring designs with the Optimization tool

## Day 4

- Using the Hierarchy Editor
- Set up and run parasitic extraction
- Backannotate extracted parasitics to the schematic
- Simulate the circuit with extracted parasitics
- Using Inherited Connections and other features of the Virtuoso Analog Design Environment

**Audience:** Analog/Mixed-Signal IC Designers  
Analog Designers

All users of the Cadence Analog Design Environment (formerly Analog Artist) 4.3x and 4.4x as well as Cadence Analog Design Environment 4.4.6 who have not yet used the WaveScan or SpectreMDL.

**Special Notes:**

**Prerequisites:** You should already have knowledge of:

UNIX OS  
Design methodology  
Analog Schematics and Simulation  
Some programming experience.

It is assumed the student has a basic knowledge of analog circuit design and terminology. It is highly recommended that the student is familiar with basic UNIX commands. It is also recommended that the student has some experience in the use of circuit simulators such as SPICE.

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