

# Low Power Implementation



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<b>Title:</b> Low-Power Implementation - v6.2	<b>Type:</b> Instructor Led Course
<b>Product Number:</b> 82145	<b>Price:</b> \$ 2,100.00
<b>Length:</b> 2 Day(s)	
<b>Category:</b> Chip Design Place and Route Flow	
<b>Description:</b> <b>This is an Engineer Explorer class for designers familiar with digital implementation using the Encounter® platform.</b>  In this course, you explore and implement several low-power techniques to reduce both dynamic and leakage power during synthesis and design implementation. You run formal verification to ensure the functionality of the low-power design.	
<b>Learning Objectives:</b> In this course, you	
	<ul style="list-style-type: none"><li>• Create and use the Si2 Common Power Format file to specify the power intent of your design.</li><li>• Set up and run synthesis directives and constraints to reduce dynamic and leakage power</li><li>• Implement multi-supply voltage (MSV) regions to reduce power consumption</li><li>• Implement a low-power clock tree</li><li>• Run concurrent timing, MSV optimization, and multi-Vt (leakage) optimization</li><li>• Implement MSV-aware detail routing</li><li>• Run sign-off power analysis with VoltageStorm® software to display the IR drop in your design.</li><li>• Verify the design implementation by running low-power formal verification</li><li>• Analyze data and debug power problems at different stages of the flow</li></ul>
<b>Software:</b> SoC Encounter™ XL Encounter® Conformal® Low Power XL	
<b>Agenda:</b> Day 1	
	<ul style="list-style-type: none"><li>• Creating power specifications using the Common Power Format file</li><li>• Exploring active and leakage power reduction concepts</li><li>• Reducing active or dynamic power during synthesis</li><li>• Optimizing for leakage power in synthesis</li></ul>
	Day 2
	<ul style="list-style-type: none"><li>• Running multi-supply voltage synthesis</li><li>• Implementing multi-supply voltage</li><li>• Optimizing leakage power during implementation</li><li>• Exploring the effective current source model</li><li>• Applying power sign-off considerations</li></ul>
<b>Audience:</b> Digital IC Designers Chip Designers ASIC Designers	
<b>Prerequisites:</b> You need to have taken the Floorplanning and Physical Synthesis with First Encounter® XL course (formerly known as First Encounter XL) and to have practical experience in	<ul style="list-style-type: none"><li>• Design methodology</li><li>• Place and route</li><li>• The SoC Encounter™ platform</li></ul>
<b>Related Courses:</b>	<a href="#">Floorplanning and Physical Synthesis with First Encounter XL</a> <a href="#">VoltageStorm Power Rail Analysis</a> <a href="#">Encounter RTL Compiler</a>

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