

# Encounter RTL Compiler



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<b>Title:</b> Encounter RTL Compiler - v7.1	<b>Type:</b> Instructor Led Course
<b>Product Number:</b> 84441	<b>Price:</b> \$ 1,400.00
<b>Length:</b> 2 Day(s)	
<b>Category:</b> Logic Design Front End Synthesis Design	
<b>Description:</b> In this course, you explore the concepts of global synthesis with the Cadence® Encounter® RTL Compiler. You learn several techniques to constrain designs, run static timing analysis, evaluate datapath logic, design for low power, and design for testability.	
<b>Learning Objectives:</b> In this course, you learn to	
	<ul style="list-style-type: none"><li>• Apply the recommended global synthesis flow using Encounter RTL Compiler.</li><li>• Navigate the design database and manipulate design objects.</li><li>• Constrain designs for global synthesis and run static timing analysis.</li><li>• Optimize RTL designs for timing and area using several strategies.</li><li>• Diagnose and analyze synthesis results.</li><li>• Use the extended datapath features of the compiler.</li><li>• Analyze and synthesize the design for low-power structures using the Common Power Format (CPF) to represent the power strategy for your design.</li><li>• Interface with other tools and place-and-route flows.</li><li>• Constrain the design for testability (optional).</li></ul>
<b>Software:</b> Encounter® RTL Compiler	
<b>Agenda:</b> <b>Day 1</b> Introduction to the Encounter RTL Compiler Synthesis flow Application of design constraints Optimization strategies  <b>Day 2</b> Synthesis of datapath structures Synthesis for low power Interface to place and route Design for testability (optional)	
<b>Audience:</b> Logic Designers Digital IC Designers ASIC Designers	
<b>Prerequisites:</b> HDL Tcl/Tk UNIX OS • You need to know the basics of ASIC Synthesis.	
<b>Related Courses:</b> <a href="#">Floorplanning and Physical Synthesis with First Encounter XL</a> <a href="#">Low-Power Implementation</a> <a href="#">Logic Equivalence Checking with Encounter Conformal EC</a>	

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