

# Allegro PCB SI GXL



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<b>Title:</b> Allegro PCB SI GXL - v16.0	<b>Type:</b> Instructor Led Course
<b>Product Number:</b> 86092	<b>Price:</b> \$ 2,100.00
<b>Length:</b> 2 Day(s)	
<b>Description:</b>	<p><b>This course was formerly called Allegro® PCB SI 630 (MGH) Signal Design. This is an Engineer Explorer class that is designed around more advanced topics and exploration of the tool.</b> This training material is intended to bring users up to speed on the technical aspects of Allegro® PCB SI GXL. This course does teach some basic tool operations. It is suggested that students who are not actively using this tool first complete either the Allegro® PCB SI Foundations course or the Allegro® Design Entry HDL SI course.</p> <p>Recent advances in silicon technology and high-speed communications have introduced buffers with data rates in the multi-Gigabit range. Simulation models need to be modeled for buffers and vias to enable accurate simulation results in this frequency range. With the Allegro PCB SI GXL tool, Cadence® Design Systems has introduced an approach to modeling and simulating these very high-speed structures. Using MacroModels, you can build buffer models that accurately operate in the multi-Gigabit range. Additionally, new algorithms have been developed to more accurately model vias.</p> <p>Among the new algorithms is a Scattering Parameters (S-Parameter) model for the vias. The behavior of this type of model can be accurately characterized over a wide frequency range. You can create and simulate both single and coupled via models. You can also use S-Parameters to model your channel interconnect from one board to another, thus facilitating the simulation of the complete serial channel through a backplane to its destination. The new Channel Analysis functionality allows you to design a channel such that the eye pattern seen at the receiver meets its requirements for eye opening and jitter.</p> <p>This training will cover all of this functionality.</p>
<b>Learning Objectives:</b>	<p>In this course you will learn to:</p> <ul style="list-style-type: none"><li>• Use MacroModels for multi-GigaHertz applications.</li><li>• Create via models using the new Via Model Generator.</li><li>• Generate S-Parameter models and perform simulation analysis using these models.</li><li>• Perform Channel Analysis to quickly run large data bit simulations and optimize your channel.</li></ul>
<b>Agenda:</b>	<p>Day One</p> <ul style="list-style-type: none"><li>• MacroModel Creation</li><li>• MacroModel Use in SigXplorer</li><li>• Pre/De-emphasis in the MacroModel</li><li>• Via Models<ul style="list-style-type: none"><li>○ Narrowband models</li><li>○ Wideband models</li><li>○ S-Parameter models</li><li>○ Coupled S-Parameter models</li></ul></li></ul> <p>Day Two</p> <ul style="list-style-type: none"><li>• S-Parameter Creation<ul style="list-style-type: none"><li>○ S-Parameter Modeling</li><li>○ S-Parameter Validation</li><li>○ Channel Loss</li></ul></li><li>• Channel Loss Channel Analysis<ul style="list-style-type: none"><li>○ High-Capacity Simulation</li><li>○ Pre-Emphasis Optimization</li><li>○ Data Rate What-Ifs Designs</li></ul></li></ul>
<b>Audience:</b>	<ul style="list-style-type: none"><li>• Digital IC Designers</li><li>• Design Engineers</li><li>• Electrical Engineers</li><li>• This course is for electrical engineers whose design responsibilities include PCB signal analysis and designers who are concerned with the problems associated with high-speed designs.</li></ul>
<b>Special Notes:</b>	You need the Allegro PCB SI GXL product version 16.0 software.
<b>Prerequisites:</b>	<ul style="list-style-type: none"><li>• Basic understanding of the UNIX or Windows operating systems and commands</li><li>• Familiarity with digital/analog circuit design methodologies</li><li>• Working knowledge of printed circuit board design and signal analysis (some SPICE simulation processes; characteristics of electro-magnetic theory; transmission line theory)</li></ul>
<b>Related Courses:</b>	<a href="#">Allegro PCB SI Foundations</a> <a href="#">Allegro Design Entry HDL SI</a>

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